Inductance and coupling of stacked vias in a multilayer superconductive IC process

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Introduction

Many advanced superconductive integrated circuit (SC IC) fabrication processes moving to multiple ground/shield layers and buried signal/power that connect through stacked vias. As gate dimensions shrink, stacked vias lead to:

- significant contributions to inductance (interesting).
- increased stray coupling (problematic and thus really interesting).

Experimental measurements of stacked via inductance have been reported [1], but not through multiple ground planes. Inductance more problematic in absence of ground sleeves around vias, because current return path becomes much more complex. Calculation requires 3D techniques. We show that InductEx can calculate inductance of stacked vias, with results verified against test structures. We also show extent of modeling required.

Coupling

Measure self inductance of SQUID loop inductor, and mutual inductance between control line and SQUID loop through modulation [4]. Cannot measure control inductance, so coupling factor is calculated with InductEx. InductEx model (55,000 segments) discretizes entire structure, except for shunt resistors. Circuit netlist extracted through 6 ports: JJs and the inputs/outputs of modulation and current line.

Via inductance

Measure self inductance of sections of SQUID through modulation [4], first \( (L_1 + L_2) \), then \( (L_1 + L_2 + 2L_{via}) \).

InductEx model (70,000 segments) again discretizes entire structure except for shunt resistors. Circuit netlist extracted through 6 ports: JJs and the inputs/outputs of modulation current line.

Experiments

We designed 5 SQUID modulation experiments to measure via inductance and coupling between lines with stacked vias in AIST ADP2 process [2].

- A: Coupling from PTL1 to PTL1.
- B: Coupling from PTL1 to PTL2.
- C: Coupling from PTL2 to PTL2.
- D: Stacked via inductance: COU-PTL1.
- E: Stacked via inductance: COU-PTL2.

Layouts use standard ADP2 cell size of 30 µm with ground pillars at centre of cell edges. InductEx, with a parameter set calibrated for ADP2 [3], is used for numerical modelling of experiments.

Results

Experimental measurements and InductEx calculations agree very well. Via inductance is significant.

Strong coupling between lines, even PTL1 to PTL2.

Other grounding options

Other grounding options investigated with InductEx.

Ground pillars next to stacked vias reduce coupling.

Ground sleeves around stacked vias reduce coupling even more.

Conclusion

Calculation models for InductEx are good - agree with measurements. We can now investigate layouts for reduced coupling numerically.

Ground pillars adjacent to stacked vias reduce stray coupling, and ground sleeves even more so. We suggest this for circuits sensitive to stray coupling in ADP2 layouts.

Table I

<table>
<thead>
<tr>
<th>Experiment</th>
<th>Parameter</th>
<th>Experimental measurements (averaged)</th>
<th>InductEx calculations</th>
</tr>
</thead>
<tbody>
<tr>
<td>A: Coupling from PTL1 to PTL1</td>
<td>( L_1 + L_2 )</td>
<td>( 5.80 , \text{pH} )</td>
<td>( 5.80 , \text{pH} )</td>
</tr>
<tr>
<td>B: Coupling from PTL1 to PTL2</td>
<td>( L_1 + L_2 )</td>
<td>( 5.09 , \text{pH} )</td>
<td>( 5.09 , \text{pH} )</td>
</tr>
<tr>
<td>C: Coupling from PTL2 to PTL2</td>
<td>( L_1 + L_2 )</td>
<td>( 6.06 , \text{pH} )</td>
<td>( 6.06 , \text{pH} )</td>
</tr>
<tr>
<td>D: Stacked via inductance: COU-PTL1</td>
<td>( L_{via} )</td>
<td>( 0.99 , \text{pH} )</td>
<td>( 0.99 , \text{pH} )</td>
</tr>
<tr>
<td>E: Stacked via inductance: COU-PTL2</td>
<td>( L_{via} )</td>
<td>( 0.89 , \text{pH} )</td>
<td>( 0.89 , \text{pH} )</td>
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</tbody>
</table>

No reliable measurement results.

Acknowledgment

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The circuits were fabricated in the the clean room for analog-digital superconductivity (CRAVITY) at National Institute of Advanced Industrial Science and Technology (AIST) with the advanced process 2 (ADP2). The AIST-ADP2 is based on the Nb circuit fabrication process developed in International Superconductivity Technology Center (STEC).

References